IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of:

Toshiyuki MOTOOKA et al.

Serial Number: 09/768,174 Group Art Unit: 2822

Filed: January 24, 2001 Examiner: J. Mitchell

For: SEMICONDUCTOR DEVICE HAVING A BALL GRID ARRAY AND A FABRICATION PROCESS THEREOF

AMENDMENT UNDER 37 CFR §1.111

Commissioner for Patents
Washington, D.C. 20231

April 3, 2002

Sir:

In response to the Office Action dated November 8, 2001, extended to April 8, 2002 by a two month Petition for Extension of Time, please amend the above-identified application as follows:

IN THE SPECIFICATION:

Amend the specification as follows:

On page 2, between lines 6 and 7, insert the following:

1. Field of the Invention

On page 2, between lines 11 and 12, insert the following:

2. Description of the Related Art

Please replace the paragraph beginning on page 5, line 13, with the following rewritten paragraph:

BRIEF DESCRIPTION OF THE DRAWINGS

Please replace the paragraph beginning on page 8, line 2, with the following rewritten paragraph:

The bonding wire 4, on the other hand, may be formed of a wire of gold or aluminum having a diameter of 25 - 30 μm and is bonded to the electrode 8a or 8b by using an ordinary wire bonding apparatus. In the present invention, a first bonding process is conducted to the electrode pad 8a on the chip, followed by a second bonding process that is conducted to the electrode pad 8b, for reducing the overall height of the semiconductor device 5.

Please replace the paragraph beginning on page 13, line 19, with the following rewritten paragraph:

In the BGA device of the present embodiment, the bonding wires 14 are used to connect the corresponding electrode pads 18a and the electrode pads 18b at a central part of the chip 12, as indicated in FIG. 8. Further, the BGA semiconductor device of the present invention is laterally surrounded by the resin potting 11.

IN THE CLAIMS:

Claims 11 and 16 have been amended as follows:

11. (Amended) A semiconductor device, comprising:

a semiconductor chip having a top surface, said semiconductor chip carrying a first electrode;

a circuit substrate attached to a top surface of said semiconductor chip, said circuit substrate carrying thereon a predetermined conductor pattern including a second electrode and a third electrode;

a solder resist layer provided on said circuit substrate;

a resin layer intervening between said top surface of said semiconductor chip and said circuit substrate;

a spherical electrode formed in an opening in said solder resist layer on said circuit substrate in correspondence to said third electrode;

a bonding wire electrically interconnecting said second electrode of said predetermined conductor pattern on said circuit substrate and said first electrode on said semiconductor chip; and

a resin potting encapsulating said bonding wire including said first and second electrodes,

said chip and said resin potting being defined by a common edge surface substantially perpendicular to a principal surface of said substrate.

16. (Amended) A semiconductor device, comprising:

a semiconductor chip having a top surface, said semiconductor chip carrying a first electrode;

a circuit substrate provided on a top surface of said semiconductor chip with a separation therefrom, said circuit substrate carrying thereon a predetermined conductor pattern including a second electrode and a third electrode;

a spherical electrode provided on said circuit substrate in correspondence to said third electrode;

a bonding wire electrically interconnecting said second electrode of said predetermined conductor pattern on said circuit substrate and said first electrode on said semiconductor chip;

a resin potting encapsulating said bonding wire including said first and second electrodes, said resin potting filling a space between said semiconductor chip and said circuit substrate; and

a resin side wall cover covering a side wall of said circuit substrate,

said chip having a side wall substantially flush to an outer surface of said resin side wall cover, said side wall of said chip being substantially perpendicular to a principal surface of said chip.

REMARKS

Claims 11-17 are pending in this application, of which claims 11 and 16 have been amended. No new claims have been added.

The Examiner has objected to the disclosure for various informalities which have been corrected in the aforementioned amendments.

Claims 11-13 and 15-18 stand under 35 USC §102(e) as anticipated by U.S. Patent 5,858,815 to Heo et al. (hereinafter "**Heo et al.**").

Applicants respectfully traverse this rejection.

Heo et al. discloses a process for manufacturing a chip size semiconductor package with a light, thin and compact structure having a reduced size of its semiconductor chip while having an increased number of pins. For the package, it is possible to use either the semiconductor chip having bond pads arranged on end portions of the chip or the semiconductor chip having bond pads arranged on the central portion of the chip. In either case, input/output terminals of the package are arranged in the form of an area array.

Figs. 2A, 4B, 5B, 6B, 7A-C, 8A, 10B, 11B and 12B show a non-conductive film 22 laminated on circuit pattern 26. As disclosed in column 5, lines 3-5, this film 22 is opened in regions where the solder balls 60 are bonded to the circuit pattern 26.

This passage suggests that the openings are formed prior to insertion of the solder balls 60, which is in contrast to the present invention, in which a solder resist layer 3b is formed on the circuit substrate 6, suggesting that liquid solder is caused to flow over layer 3b and the openings help form

the connections of the solder balls to the circuit substrate electrodes. **Heo et al.** fails to specifically disclose that non-conductive film 22 consists of a solder resist material.

Accordingly, claim 11 has been amended to recite this distinction.

Furthermore, **Heo et al.** fails to disclose that the substrate is lifted up from the chip after it is placed on the chip, as shown in FIGS. 10-11F of the instant application

Because the circuit substrate is supported by the potting resin not only at the bottom surface but also at the sidewall, the circuit substrate is held stably in the scribing process shown in FIG. 11F of the instant application. As a result, it is possible to avoid chipping of the semiconductor chip.

Accordingly, claim 16 has been amended to recite this distinction, and the 35 USC §102(e) rejection should be withdrawn.

Claim 14 stands rejected under 35 USC §103(a) as unpatentable over **Heo et al.** in view of U.S. Patent 5,729,051 to Nakamura (hereinafter "**Nakamura**").

Applicants respectfully traverse this rejection.

Nakamura discloses a tape automated bonding type semiconductor device having a glass epoxy substrate 7 but, like **Heo et al.**, fails to teach, mention or suggest the solder resist layer recited in the proposed amendments to claim 11, from which claim 14 depends.

Thus, the 35 USC §103(a) rejection should be withdrawn.

In view of the aforementioned amendments and accompanying remarks, claims 11-17, as amended, are in condition for allowance, which action, at an early date, is requested.

Attached hereto is a marked-up version of the changes made to the specification and claims

by the current amendment. The attached page is captioned "**VERSION WITH MARKINGS TO SHOW CHANGES MADE**".

If, for any reason, it is felt that this application is not now in condition for allowance, the Examiner is requested to contact Applicants' undersigned attorney at the telephone number indicated below to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed, Applicants respectfully petition for an appropriate extension of time. The fees for such an extension or any other fees which may be due with respect to this paper, may be charged to Deposit Account No. 01-2340.

Respectfully submitted,

ARMSTRONG, WESTERMAN & HATTORI, LLP

William L. Brooks
Attorney for Applicants
Reg. No. 34,129

Atty. Docket No. 980100A
Suite 1000
1725 K Street, N.W.
Washington, D.C. 20006
Tel: (202) 659-2930
WLB:ylw
Enclosures: Version With Markings To Show Changes Made
Q:\FLOATERS\WLB\980100a amendment